

What is Claimed is:

- 1 1. An apparatus, comprising:
 - 2 a first circuit, disposed within an integrated circuit, the first circuit having a first
 - 3 positive supply rail coupled to an output terminal of a regulated power supply, the first
 - 4 circuit having at least one operating characteristic that is dependent upon the
 - 5 magnitude of a voltage that is supplied at the output terminal of the regulated power
 - 6 supply, the first circuit operable to provide a first signal indicative of the at least one
 - 7 operating characteristic at a first output terminal; and
 - 8 a second circuit coupled to the first output terminal of the first circuit, the second
 - 9 circuit adapted to receive a reference clock signal, the second circuit further adapted to
 - 10 compare the first signal and the reference clock signal and to provide a control signal
 - 11 for controlling the magnitude of the voltage that is supplied at the output terminal of the
 - 12 regulated power supply;
 - 13 wherein the regulated power supply, responsive to the second signal, increases
 - 14 or decreases the magnitude of the voltage that is supplied at the output terminal of the
 - 15 regulated power supply, such that at least one operating characteristic of the first circuit
 - 16 is modified to be within a predetermined range.
- 1 2. The apparatus of Claim 1, wherein the first circuit comprises a inverter chain.
- 1 3. The apparatus of Claim 1, wherein the first circuit comprises a ring oscillator.

1 4. The apparatus of Claim 1, wherein the second circuit is disposed within the
2 integrated circuit.

1 5. The apparatus of Claim 1, wherein the regulated power supply includes a
2 plurality of circuit elements that are disposed external to the integrated circuit.

1 6. The apparatus of Claim 5, wherein the plurality of circuit elements is disposed
2 within a package that houses the integrated circuit.

1 7. The apparatus of Claim 1, wherein the at least one operating characteristic of
2 the first circuit is speed.

1 8. The apparatus of Claim 1, wherein the at least one operating characteristic of
2 the first circuit is leakage current.

1 9. The apparatus of Claim 1, further comprising a third circuit, coupled to the
2 second circuit, the third circuit adapted to provide a signal indicative of the resistivity of
3 at least one conductor that is disposed within the integrated circuit.

1 10. The apparatus of Claim 1, further comprising a third circuit, coupled to the
2 second circuit, the third circuit adapted to store a history of the control signals provided
3 for controlling the magnitude of the voltage that is supplied at the output terminal of the
4 regulated power supply.

1 11. The apparatus of Claim 1, wherein the integrated circuit is a field programmable
2 gate array.

1 12. A method of operating an electronic product, comprising:

2 a) operating a first voltage regulator to produce a first voltage at an output
3 thereof;

4 b) determining whether a first voltage dependent characteristic of a first circuit,
5 the first circuit receiving the first voltage, is within a predetermined range;

6 c) generating, if the determination of (b) is negative, at least one control signal,
7 and communicating the at least one control signal to the first voltage regulator; and

8 d) modifying, responsive to the at least one control signal, the operation of the
9 first voltage regulator to produce a second voltage at the output thereof;

10 wherein the first circuit is disposed within an integrated circuit.

1 13. The method of Claim 12, further comprising:

2 e) determining whether the first voltage dependent characteristic of the first
3 circuit, is within the predetermined range;

4 f) generating, if the determination of (e) is negative, at least one control signal,
5 and communicating the at least one control signal to the first voltage regulator; and

6 g) modifying, responsive to the at least one control signal, the operation of the
7 first voltage regulator to produce a third voltage at the output thereof.

1 14. The method of Claim 13, wherein the first voltage dependent characteristic is
2 selected from the group consisting of switching speed and leakage current.

1 15. The method of Claim 13, wherein the first voltage dependent characteristic is
2 selected from the group consisting of FET drive current, and FET leakage current.

1 16. The method of Claim 13, further comprising:

2 h) operating a second voltage regulator to produce a third voltage at an output
3 thereof;

4 i) determining whether a second voltage dependent characteristic of a first
5 circuit, the first circuit receiving the third voltage, is within a predetermined range;

6 j) generating, if the determination of (i) is negative, at least one control signal,
7 and communicating the at least one control signal to the second voltage regulator; and

8 k) modifying, responsive to the at least one control signal, the operation of the
9 second voltage regulator to produce a fourth voltage at the output thereof.

1 17. The method of Claim 16, wherein the output of the first voltage regulator
2 provides a positive voltage supply to the first circuit, and wherein the second voltage
3 regulator provides substrate bias to the first circuit.

1 18. The method of Claim 13, further comprising storing a history of the control
2 signals provided to the first voltage regulator.

1 19. The method of Claim 13, further comprising comparing the control signals
2 provided to the first voltage regulator to a predetermined threshold.

1 20. The method of Claim 19, further comprising:
2 determining whether the control signals provided to the first voltage regulator
3 exceed the predetermined threshold; and
4 generating, if the determination is affirmative, a signal indicating that service is
5 required.

1 21. The method of Claim 19, further comprising:
2 receiving information indicating the temperature at which the integrated circuit is
3 operating; and
4 modifying, responsive to the temperature information, the predetermined
5 threshold.

1 22. The method of Claim 12, wherein the integrated circuit is a field programmable
2 gate array.